

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

METHOD FOR REDUCING SHALLOW TRENCH ISOLATION
CONSUMPTION IN SEMICONDUCTOR DEVICES

Application Number :

Confirmation Number:

First Named Applicant: Bruce Doris

Attorney Docket Number: FIS920030256US1

Art Unit:

Examiner:

Search string: (5960276 or 6146970 or 6194285 or 6214698 or 6437417 or 6492220 or 6498383
or 6514833 or 6576558 or 20020064967 or 20020102793).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5960276	1999-09-28	Liaw, et al.			
	2	6146970	2000-11-14	Witek, et al.			
	3	6194285	2001-02-27	Lin et al.			
	4	6214698	2001-04-10	Liaw, et al.			
	5	6437417	2002-08-20	Gilton			
	6	6492220	2002-12-10	Ikeda			
	7	6498383	2002-12-24	Beyer, et al.			
	8	6514833	2003-02-04	Ishida, et al.			
	9	6576558	2003-06-10	Lin et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20020064967	2002-05-30	Whitman, et al.			
	2	20020102793	2002-08-01	Wu			

Signature

Examiner Name

Date